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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/593,830	09/22/2006	Hisao Igarashi	296431US2PCT	5607
22850	7590	02/26/2008		
OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314				
EXAMINER				
TANG, MINH NHUT				
ART UNIT		PAPER NUMBER		
2829				
NOTIFICATION DATE		DELIVERY MODE		
02/26/2008		ELECTRONIC		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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# Office Action Summary

**Application No.**

10/593,830

**Applicant(s)**

IGARASHI ET AL.

**Examiner**

Minh N. Tang

**Art Unit**

2829

**Period for Reply** -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 22 September 2006.  
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-12 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-4 and 9-12 is/are rejected.  
7) ☒ Claim(s) 5-8 is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 22 September 2006 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☒ Information Disclosure Statement(s) (PTO/SB/003)  
Paper No(s)/Mail Date 9/22/06  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_  
5) ☐ Notice of Informal Patent Application  
6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

***Priority***

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

***Information Disclosure Statement***

2. The information disclosure statement (IDS) submitted on September 22, 2006 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

***Drawings***

3. Figure 17 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Specification***

4. The Preliminary Amendment received on September 22, 2006 has been entered.
5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is

requested in correcting any errors of which applicant may become aware in the specification.

### ***Claim Objections***

6. Claims 2-9 are objected to because of the following informalities:

a/ in claim 2, a limitation followed by linking terms (e.g., can be, preferably, maybe, for instance, especially) is considered indefinite since the resulting claim does not clearly set forth the metes and bounds of the patent protection desired. Therefore, "can be" (line 4) should be -- is --.

b/ in claim 9, since claim 9 is an independent claim which includes any one of claims 1 to 8, therefore Applicant is advised that should claim 9 including claim 8 be found allowable, claims 9 including any one of claims 1-7 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

c/ claims 3-8 are objected since they depend on objected base claim.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-4 and 9-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Kasukabe et al. (U.S.P. 6,305,230).

As to claims 1 and 9-10, Kasukabe et al. disclose, in Figs. 1, 6 and 9, a probe device suitable for use in conducting electrical inspection of a great number of integrated circuits (2, Fig. 1) formed on a wafer (1, Fig. 1), which comprises: a circuit board for inspection (44, Fig. 9) having a great number of inspection electrodes (69, Fig. 9) on a front surface (lower surface) thereof; a probe card (61, 62, 47, Fig. 9) having a circuit board for connection (61), on the back surface (upper surface) of which a plurality of terminal electrodes (62) have been formed in accordance with a pattern corresponding to a pattern of the inspection electrodes (69) of the circuit board for inspection (44), and a contact member (47), which is provided on a front surface (lower surface) of the circuit board for connection (61), and on which a great number of contacts (also called 47) brought into contact with respective electrodes (3, Fig. 1) to be inspected of the integrated circuits (2) on the wafer (1), which is an object of inspection, are arranged, in which the respective terminal electrodes (62) of the circuit board for connection (61) are arranged so as to be opposed to the inspection electrodes (69) of the circuit board for inspection (44); an anisotropically conductive connector (70, Fig. 9), which is arranged between the circuit board for inspection (44) and the circuit board for connection (61) in the probe card (61, 62, 47), and electrically connects the respective inspection electrodes (69) to the respective terminal electrodes (62) by being pinched by the circuit board for inspection (44) and the circuit board for connection (61); and a parallelism adjusting mechanism (42, 55, Fig. 6) for adjusting a parallelism of the circuit

board for inspection (44) to the wafer (1) and a parallelism of the circuit board for connection (61) to the wafer (1), wherein the parallelism adjusting mechanism (42, 55) is equipped with a location-varying mechanism (43, 58, Fig. 6), which relatively displaces the circuit board for inspection (44) or the circuit board for connection (61) in a thickness-wise direction of the anisotropically conductive connector (70).

As to claim 2, Kasukabe et al. disclose in Figs. 1, 6 and 9, the parallelism adjusting mechanism (42, 55) is equipped with a plurality of location-varying mechanisms (43, 58), and each of the location-varying mechanisms (43, 58) is so constructed that the quantity of displacement of the circuit board for inspection (44) or the circuit board for connection (61) is set independently of each other.

As to claim 3, Kasukabe et al. disclose in Figs. 1, 6 and 9, spacers (i.e., thickness of anisotropic 70) for regulating the deformation quantity of the anisotropically conductive connector (70) are provided between the circuit board for inspection (44) and the circuit board for connection (61) in the probe card (61, 62, 47).

As to claim 4, Kasukabe et al. disclose in Figs. 1, 6 and 9, the overall thickness of the spacer (thickness of anisotropic 70) is at least 50% of the overall thickness of the anisotropically conductive connector (70).

As to claim 11, Kasukabe et al. disclose in Figs. 1, 6 and 9, the parallelism adjusting mechanism (42, 55) is equipped with a plurality of location-varying mechanisms (43, 58), electric resistance values of the respective conductive parts for connection in the anisotropically conductive connector (70) are measured in a state that the contact member (47) in the probe card (61, 62, 47) is brought into contact with the

wafer (1), and the correction quantity of the quantity of displacement by the respective location-varying mechanisms (43, 58) is set in such a manner that the distribution of the resultant electric resistance values becomes an even state.

As to claim 12, Kasukabe et al. disclose in, for example, column 7, lines 49-57, the inspection initial state is set in such manner that the respective electrical resistance values of the conductive parts for connection in the anisotropically conductive connector are at most  $0.1\Omega$ , and a load per one conductive part for connection in the anisotropically conductive connector (70) is 0.01 to 0.4 N.

***Allowable Subject Matter***

9. Claims 5-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
10. The following is a statement of reasons for the indication of allowable subject matter:

Claims 5-8 recite, inter alia, the anisotropically conductive connector is composed of a frame plate, in which a plurality of anisotropically conductive film-arranging holes each extending in a thickness-wise direction of the frame plate have been formed corresponding to electrode regions, in which electrodes intended to be connected in the circuit board for connection and the circuit board for inspection have been arranged, and a plurality of elastic anisotropically conductive films arranged in the respective anisotropically conductive film-arranging holes in this frame plate and each supported by the peripheral edge of the anisotropically conductive film-arranging hole,

Art Unit: 2829

and wherein the spacers are arranged on both sides of the frame plate in the anisotropically conductive connector, and the spacers are each in the form of a frame, in which openings are formed in regions corresponding to the regions where the elastic anisotropically conductive films in the anisotropically conductive connector have been formed, and have finely projected portions each composed of an elastic member on at least contact surfaces with the circuit board for inspection and contact surfaces with the circuit board for connection.

The art of record does not disclose the above limitations, nor would it be obvious to modify the art of record so as to include the above limitations.

***Prior Art Of Record***

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Nakata	6,215,321	Probe Card For Wafer-Level Measurement, Multilayer Ceramic Wiring Board, And Fabricating Methods Therefor.
Nakata et al.	6,297,658	Wafer Burn-In Cassette And Method Of Manufacturing Probe Card For Use Therein.
Johnson	2002/0196046	Method And Apparatus For Wafer Scale Testing.



***Communication***

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh N. Tang whose telephone number is (571) 272-1971. The examiner can normally be reached on M-Th (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha T. Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Minh N. Tang/ 02/15/08  
Minh N. Tang  
Primary Examiner  
Art Unit 2829